REMARKS

In the foregoing amendments, claims 16-18 were added to the application. These claims define that the notch has a shape so that a secluded portion of the inner wall face will not contact a member inserted into the notch for orienting the semiconductor wafer, and the markings are formed on the secluded portion of the inner wall face. Support for these claims can be found in figure 2 and the accompanying discussion in applicant's specification disclosure. Accordingly, claims 1-18 are in the application for consideration by the examiner.

The Official action set forth two different prior art rejections of applicant's claims. Claims 1 and 8-15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patent No. 4,418,467 of Iwai in view of U.S. patent No. 5,028,200 of Shimane in further view of U.S. patent No. 4,327,292 of Wang *et al.* (Wang). This rejection begins at the bottom of page 2 and continues to the bottom of page 7. The teachings of Iwai and Wang were previously cited against applicant's claims. The teachings of Shimane were newly cited against applicant's claims. The rejection is set forth from the bottom of page 7 through the middle of page 9 of the Official action.

Claims 2-7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Iwai, Shimane, and Wang in further view of U.S. patent No. 6,400,405 of Oishi *et al.* (Oishi). The teachings of Oishi were previously cited against

applicant's claims.

Applicant respectfully submits that the teachings of Iwai, Shimane, and Wang either alone, together, or combined with the teachings of Oishi do not disclose or suggest the invention as set forth in present claims 1-18 within the meaning of 35 U.S.C. § 103.

The teachings of Iwai were used as a primary reference in all of the prior art rejections, and thus form the cornerstone of all the rejections against applicant's claims. The teachings of Iwai propose a technology where markings are formed on the peripheral exposed edge of the wafer, as shown in figure 11 therein. The presently claimed invention is directed to a system for marking wafers that overcomes the deficiencies in the technology proposed by Iwai. During the semiconductor wafer-fabrication process, the semiconductor wafer receives various mechanical impacts from gripping mechanisms used by robots (such as the waffer positioning mechanism proposed by Shimane). In addition, the semiconductor wafer is subjected to various processing steps including mechanical, chemical, combined mechanical and chemical, chamfering, lapping, etc. The mechanical impacts cause scratching, cracking or chipping of the semiconductor wafer, and the processing steps removed outer or exposed portions of the semiconductor wafer. Thus, if markings were formed on the peripheral exposed edge of the wafer, as shown in figure 11 of Iwai, the character or legibility of the markings will diminish as a result of the

scratching, cracking, chipping resulting from mechanical impacts and the removal of outer or exposed portions of the semiconductor wafer of the semiconductor wafer resulting from the processing steps.

The presently claimed invention overcomes the deficiencies of markings formed on the peripheral exposed edge of the wafer as proposed by Iwai. The presently claimed invention is directed to a semiconductor wafer having an outer peripheral face containing a notch having an inner wall face extending inwardly and away from the outer peripheral face of the semiconductor wafer towards a center of the semiconductor wafer, wherein markings made from dot marks respectively having a maximum length of 1 to 13 μm are formed on the inner wall face.

In contrast to applicant's claims, the markings proposed by Iwai will most likely disappear from mechanical impacts and/or polishing steps, during the fabrication of the wafer. Due to the location of the markings in the presently claimed invention, the markings are hardly influenced by aforementioned mechanical impacts of scratching, cracking or chipping of the semiconductor wafer, and the processing steps of removing outer or exposed portions of the semiconductor wafer. Thus, the structure of the presently claimed semiconductor wafer and the arrangement of the markings thereon maintains the character and legibility of the markings at stages (or steps) along the semiconductor wafer-fabrication process.

Since the teachings of Iwai propose a technology where markings are formed on the peripheral exposed edge of the wafer, as shown in figure 11 therein, these teachings cannot possibly motivate one of ordinary skill in the art to the presently claimed invention.

The teachings of Shimane do not cure or rectify the deficiencies in the teachings of Iwai. The teachings of Shimane are directed to a positioning mechanism for notched wafers. See, for example, figures 3 and 4 of Shimane where a notch in a semiconductor wafer is used to orient the wafer. The Official action took the position that would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Iwai by using the shape of the notch as taught by Shimane. The Official action continued that the ordinary artisan would have been motivated to modify Iwai in the manner described above for at least the purpose of producing more integrated circuit chips, citing column 2, lines 10-18, of Shimane. Applicant respectfully submits that this conclusion of obviousness over the combined teachings of Iwai and Shimane, together with Wang and/or Oishi, constitutes an unsupported, arbitrary and erroneous legal conclusion of obviousness. Applicant respectfully submits that such an impermissible combination of references cannot establish a *prima facie* case of obviousness within the meaning of 35 U.S.C. §103. See, for example, *In re Wesslau*, 147 USPQ 391, (CCPA 1965).

As mandated in *Ashland Oil Company, Inc. v. Delta Resins Factories*, 227 USPQ 657, 667 (Fed. Cir. 1985), the decision maker must provide a factual basis for the legal conclusion of obviousness as follows:

> To properly combine references A and B to reach the conclusion that the subject matter of a patent would have been obvious, case law requires that there be some teaching, suggestion, or inference in either reference A or B or both, or knowledge generally available to one of ordinary skill in the relevant art, which would have lead one skilled in the art to combine the relevant teachings of references A and B. [citations omitted] The decision maker's determination as to what objective evidence in reference A or B, or both, or knowledge generally available to one of ordinary skill in art is the nature of a factual finding.
>
> The decision maker, however, after making findings as to the objective evidence, must subjectively analyze these factual findings to determine whether the teachings of references A and B could have been combined. Thus, the ultimate determination as to whether references could have been combined is a legal conclusion.

The *Ashland Oil* court also obligated the decision maker to explain the decision, by setting forth the teachings from the references that were relied on as a factual basis in reaching the conclusion of obviousness. The Court stated:

> The District Court did not elucidate any factual teachings, suggestions, or incentives from this prior art that show the propriety of combination, nor in fact did the District Court even point out what teachings from each of the references, when considered in combination, were relied upon in concluding that the invention of claim 10 would have been obvious. Nor apparently did the District Court give any consideration to teachings in those references which would have lead one of ordinary skill in the art away from the invention of claim 10. We would have to say that the District Court used claim 10 of the '797 Patent as a blue print and abstracted individual teachings from the Rothrock patent, Megson, and Maktin to create the Pep resin of claim 10. [citation omitted] <u>This was error as a matter of law.</u> (emphasis added)

In support of the above, the Court cited the cases of *ACS Hospital Systems v. Montefiore Hospital*, 221 USPQ 929, 933 (Fed. Cir. 1985); *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 220 USPQ 303, 311, 312 (Fed. Cir. 1983); and *In re Sernaker*, 217 USPQ 1, 5 (Fed. Cir. 1983), which have frequently been cited by the Federal Circuit for supporting the above well-established principles.

There is absolutely no motivation in the combination of Iwai and Shimane, together with Wang and/or Oishi, for one of ordinary skill in the art to provide the markings made from dot marks having a maximum length of 1 to 13 μm on the inner wall face of a notch having an inner wall face extending inwardly and away from the outer peripheral face of the semiconductor wafer towards a center of the semiconductor wafer, as required in the present claims. The problems associated with the interaction between the inner wall face of the notch of a semiconductor wafer and a pin or protrusion (such as protrusion 7 in figure 4 of Shimane), when used in conjunction with the notch to orient the semiconductor wafer, are discussed in the applicant's specification disclosure at, for example, page 8, line 15, to page 10, line 5; page 13, lines 5-24; and elsewhere. This discussion in applicant's specification disclosure demonstrates that one of ordinary skill in the art would not be motivated to provide the markings on the inner wall face of a notch, such as proposed by Shimane, due to the problems associated with scratching the markings, etc.

Applicant respectfully submits that the rejection of the present claims

does not elucidate any factual teachings, suggestions or incentives from the teachings of Iwai and Shimane, together with Wang and/or Oishi to show the propriety of the combination of these teachings. Further, the Official action has not given any consideration to the teachings in these references that would have lead one skilled in the art away from the invention as defined in the present claims. Accordingly, applicant respectfully submits that the examiner has not complied with the mandate set forth in *Ashland Oil.* Moreover, the examiner has failed to satisfy his burden of establishing a *prima facie* case of obviousness by showing some objective teaching or generally available knowledge that would lead one skilled in the art to combine the teachings of the cited references. See *In re Fine*, 5 USPQ2d 1596 (Fed. Cir. 1988). For such reasons, applicant respectfully submits that the rejection of the present claims under 35 U.S.C. §103 over the combined teachings of Iwai and Shimane, together with Wang and/or Oishi constitutes an unsupported, arbitrary and erroneous legal conclusion of obviousness. Therefore, applicant respectfully requests that the examiner reconsider and withdraw all the prior art rejection set forth in the outstanding Office action.

New claims 16-18 further distinguish applicant's claimed invention from other cited references by defining that the notch has a shape so that a secluded portion of the inner wall face will not contact a member inserted into the notch for orienting the semiconductor wafer, and the markings are formed on the secluded portion of the inner wall face. The teachings of Shimane, which are

the only teachings cited against the present claims that propose a notch, do not contemplate or suggest this claimed structure.

The teachings of Oishi and Wang do not cure or rectify the afore-mentioned deficiencies in the teachings of Iwai and Shimane. It appears that figure 3 of Wang simply proposes the alignment of patterns 38 and 20 of the masked together with the wafer 36. The teachings of Oishi were discussed and distinguished from applicant's claimed invention in the previous response filed on March 31, 2003, which comments are incorporated herein by reference.

For the foregoing reasons, applicant respectfully submits that none of the teachings of Iwai, Shimane, Wang and/or Oishi, either taken alone or in combination contemplate or suggest the invention as set forth in any of the present claims within the meanings of 35 USC § 102 or 35 USC § 103. Therefore, applicant respectfully requests that the examiner reconsider and withdraw all the prior art rejections of applicant's claims in the outstanding Office action.

It is respectfully noted that the Official action sets forth some comments concerning the limitations in applicant's claims as product-by-process language. Applicant is not requesting that the examiner make any determination or consideration that is not in accordance with all the case law cited in the outstanding Office action. In patent claims, the structure of an invention can be defined by the process of making the structure. For example, a clean dish has a structure that is different from a dish soiled with food, and a

frosted glass has a structure different from a non-frosted glass. Along these same lines, the process limitation set forth in applicant's claims define a semiconductor wafer having a specific structure. Considering applicant's claims, it is respectfully noted that applicant's claim 12 defines when the markings are arranged on the inner surface of the notch prior to various fabrication steps. For example, this claim defines the semiconductor at a point in time, mainly, before fabrication, when the markings were provided on the semiconductor. In order for the prior art to render such a claim obvious, prior art would have to show a semiconductor wafer that had or has markings on the inner surface of the notch before processing of the semiconductor wafer. If such a semiconductor wafer was subjected to later fabrication steps, the appearance of the markings will change due to such fabrication steps. The applicant cannot find such structure in the teachings of the cited prior art.

Applicant's claim 13 defines that the markings contained all the history information concerning the fabrication steps for fabricating the semiconductor wafer. This claim defines the information contained in the markings identifies all the fabrication steps used when fabricating the wafer. Applicant cannot find any discussion in the cited teachings concerning this aspect of the presently claimed invention.

Applicant's claim 14 defines a marked semiconductor made from a semiconductor wafer that was subjected to at least one fabrication step that is visibly discernable on the marked semiconductor wafer. This claim defines a

semiconductor that was marked prior to at least one fabrication step at a time, after the fabrication step(s) were completed, and requires that the markings are still present. In other words, this claim defines a wafer having markings thereon that have survived fabrication step(s). The applicant cannot find this structure in the prior art cited in the outstanding Office action.

Claim 15 includes language similar to that of claim 14. Claim 15 defines that the peripheral surface of the semiconductor wafer contains visibly discernable structure resulting from processing steps. Such processing steps can include cleaning, polishing, slicing, etc. There is a difference in structure between a cleaned and an uncleaned wafer, a polished and an unpolished wafer, and a sliced and an unsliced wafer; the same as there is a difference between a clean plate and a plate soiled with food. Thus, these limitations in applicant's claims concerning visibly discernible structure resulting from processing steps define physical limitations that can be observed visually and/or touched. These are the limitations that the applicant found necessary to properly define the present invention. Since the cited prior art does not show these limitations, the cited prior art cannot establish a *prima facie* case of obviousness against applicant's claims within the meaning of 35 U.S.C. §103. Therefore, applicant respectfully requests that the examiner reconsider and withdraw all the rejections of the present claims.

In view of the foregoing amendments and remarks, applicant respectfully submits that claims 1-18 are in condition for allowance. Accordingly, a formal

allowance of these claims is respectfully requested.

The foregoing is believed to be a complete and proper response to the Official action mailed October 8, 2003. While it is believed that all the claims in this application are in condition for allowance, should the examiner have any comments or questions, it is respectfully requested that the undersigned be telephoned at the below listed number to resolve any outstanding issues.

In the event this paper is not timely filed, applicant hereby petitions for an appropriate extension of time. The fee therefor, as well as any other fees which become due, may be charged to our deposit account No. 22-0256.

Respectfully submitted,
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